74CBTLV3306

2-bit bus switch

Rev. 1 — 7 December 2016 | Product data sheet

1. General description

The 74CBTLV3306 is a 2-bit high-speed bus switch with separate output enable inputs ($n\overline{OE}$). Each switch is disabled when the associated output enable ($n\overline{OE}$) input is HIGH.

To ensure the high-impedance OFF-state during power-up or power-down, $n\overline{OE}$ should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
- 4 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3306DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74CBTLV3306GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74CBTLV3306DC	b6
74CBTLV3306GT	b6

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

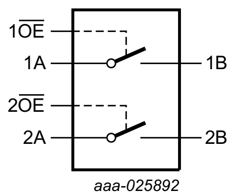


Fig 1. Logic symbol

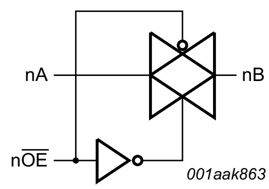


Fig 2. Logic diagram (one switch)

6. Pinning information

6.1 Pinning

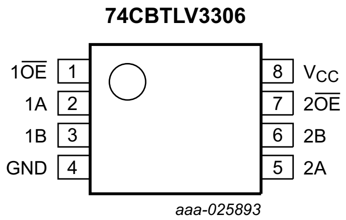


Fig 3. Pin configuration SOT765-1

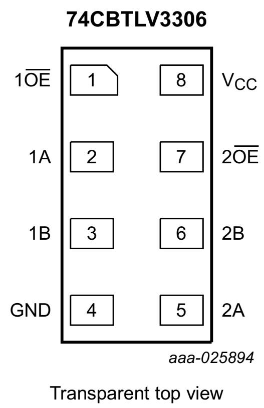


Fig 4. Pin configuration SOT833-1

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 7	output enable input
1A, 2A	2, 5	data input/output (A port)
1B, 2B	3, 6	data input/output (B port)
GND	4	ground (0 V)
V_{CC}	8	positive supply voltage

7. Functional description

Table 4. Function selection[1]

Input	Input/output
$n\overline{OE}$	**nA, nB**
L	nA = nB
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
V_I	input voltage	control inputs [1]	–0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode [2]	–0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < –0.5 V	–50	-	mA
I_{SK}	switch clamping current	V_I < –0.5 V	–50	-	mA
I_{SW}	switch current	V_{SW} = 0 V to V_{CC}	-	±128	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		–100	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

[3] For VSSOP8 packages: above 110 °C, the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage	control inputs	0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T_{amb}	ambient temperature		–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	pin $n\overline{OE}$; V_{CC} = 2.3 V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I_I	input leakage current	pin $n\overline{OE}$; V_I = GND to V_{CC}; V_{CC} = 3.6 V	-	-	±1.0	-	±20	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 3.6 V; see Figure 5	-	-	±1	-	±20	μA

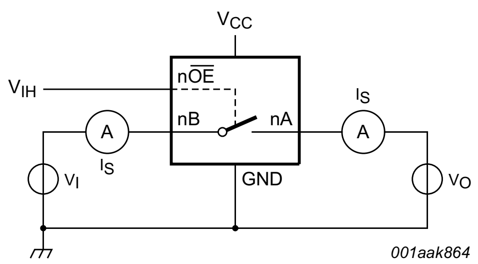
Table 7. Static characteristics *...continued*
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 3.6 V; see Figure 6		-	-	±1	-	±20	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±10	-	±50	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{SW} = GND or V_{CC}; V_{CC} = 3.6 V		-	-	10	-	50	µA
ΔI_{CC}	additional supply current	pin $n\overline{OE}$; V_I = V_{CC} – 0.6 V; V_{SW} = GND or V_{CC}; V_{CC} = 3.6 V	[2]	-	-	300	-	2000	µA
C_I	input capacitance	pin $n\overline{OE}$; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V		-	0.9	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V		-	3.0	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V		-	10.6	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

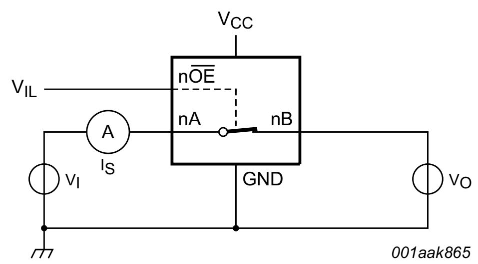
[2] One input at 3 V, other inputs at V_{CC} or GND.

10.1 Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig 5. Test circuit for measuring OFF-state leakage current (one switch)



V_I = V_{CC} or GND and V_O = open circuit.

Fig 6. Test circuit for measuring ON-state leakage current (one switch)

10.2 ON resistance

Table 8. Resistance R_{ON}

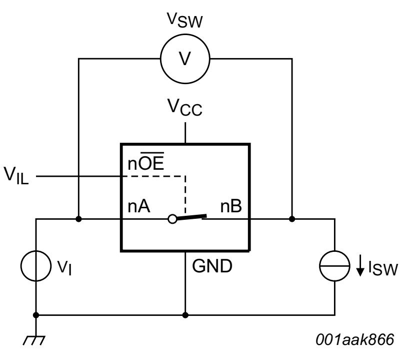
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R_{ON}	ON resistance	V_{CC} = 2.3 V to 2.7 V; see Figure 8 to Figure 10 [2]						
		I_{SW} = 64 mA; V_I = 0 V	-	3.6	8.0	-	15.0	Ω
		I_{SW} = 24 mA; V_I = 0 V	-	3.6	8.0	-	15.0	Ω
		I_{SW} = 15 mA; V_I = 1.7 V	-	6.6	40.0	-	60.0	Ω
		V_{CC} = 3.0 V to 3.6 V; see Figure 11 to Figure 13						
		I_{SW} = 64 mA; V_I = 0 V	-	3.5	7.0	-	11.0	Ω
		I_{SW} = 24 mA; V_I = 0 V	-	3.5	7.0	-	11.0	Ω
		I_{SW} = 15 mA; V_I = 2.4 V	-	4.6	15.0	-	25.5	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

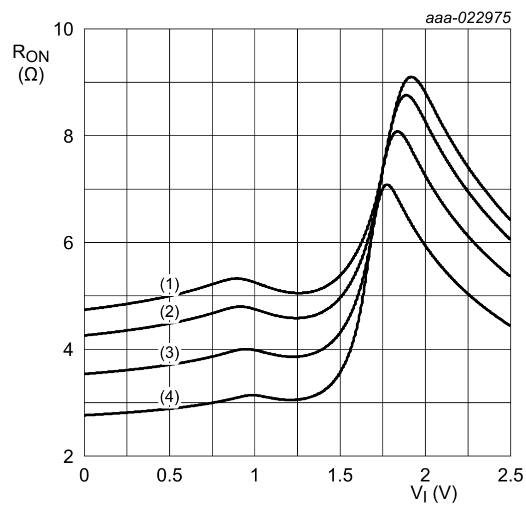
[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

10.3 ON resistance test circuit and graphs



$R_{ON} = V_{SW} / I_{SW}$.

Fig 7. Test circuit for measuring ON resistance (one switch)



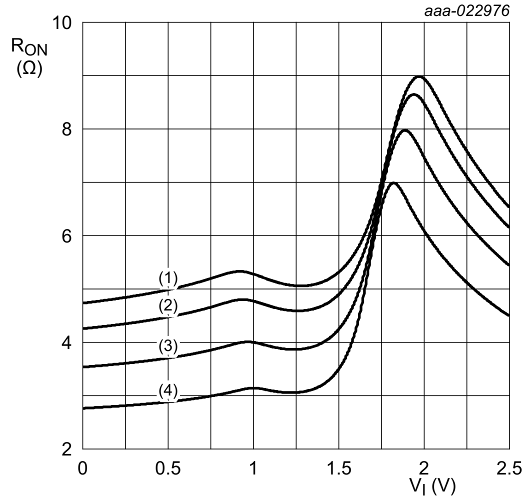
(1) T_{amb} = 125 °C.

(2) T_{amb} = 85 °C.

(3) T_{amb} = 25 °C.

(4) T_{amb} = –40 °C.

Fig 8. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 15 mA



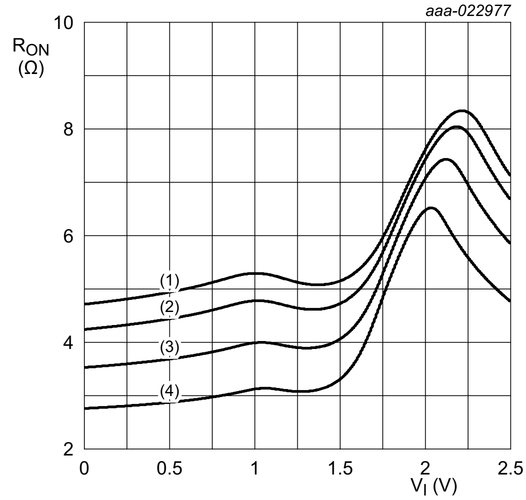
(1) T_{amb} = 125 °C.

(2) T_{amb} = 85 °C.

(3) T_{amb} = 25 °C.

(4) T_{amb} = −40 °C.

Fig 9. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 24 mA



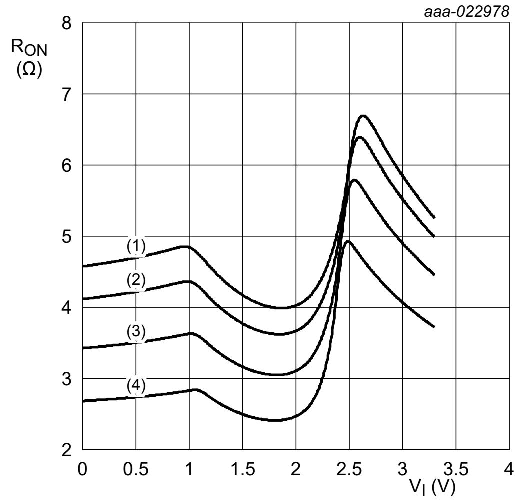
(1) T_{amb} = 125 °C.

(2) T_{amb} = 85 °C.

(3) T_{amb} = 25 °C.

(4) T_{amb} = −40 °C.

Fig 10. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 64 mA



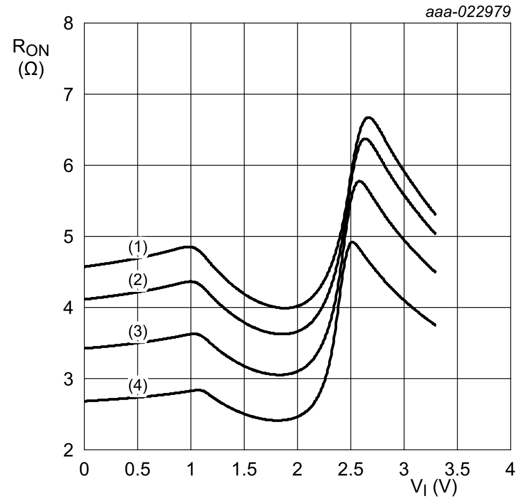
(1) T_{amb} = 125 °C.

(2) T_{amb} = 85 °C.

(3) T_{amb} = 25 °C.

(4) T_{amb} = −40 °C.

Fig 11. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 15 mA



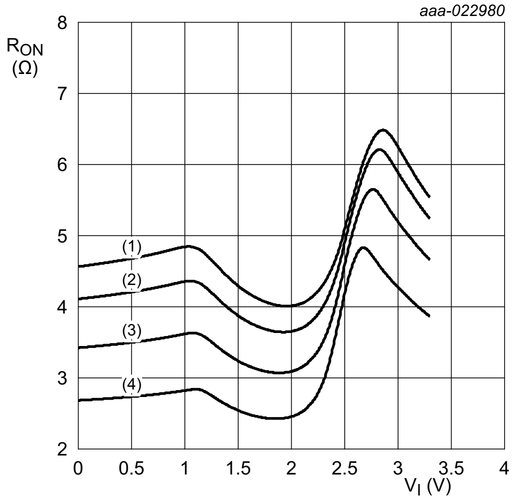
(1) T_{amb} = 125 °C.

(2) T_{amb} = 85 °C.

(3) T_{amb} = 25 °C.

(4) T_{amb} = −40 °C.

Fig 12. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 24 mA



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = –40 °C.

Fig 13. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 64 mA

11. Dynamic characteristics

Table 9. Dynamic characteristics
GND = 0 V; for test circuit see Figure 16

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nB or nB to nA; see Figure 14	[2][3]						
		V_{CC} = 2.3 V to 2.7 V		-	-	0.13	-	0.20	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	0.20	-	0.31	ns
t_{en}	enable time	$n\overline{OE}$ to nA or nB; see Figure 15	[4]						
		V_{CC} = 2.3 V to 2.7 V		1.0	2.7	4.6	1.0	6.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.4	4.4	1.0	6.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nA or nB; see Figure 15	[5]						
		V_{CC} = 2.3 V to 2.7 V		1.0	2.2	3.9	1.0	5.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.9	4.2	1.0	5.5	ns

[1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.

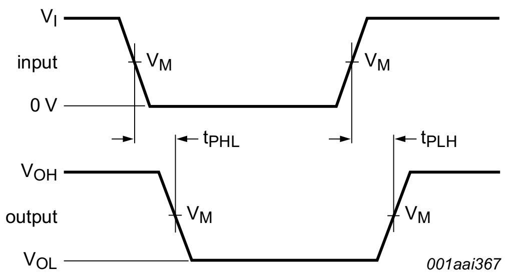
[2] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

[3] t_{pd} is the same as t_{PLH} and t_{PHL}.

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

12. Waveforms



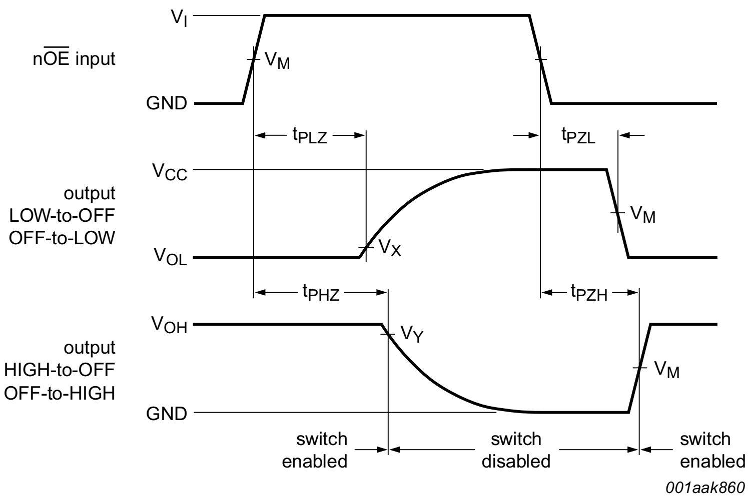
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. The data input (nA or nB) to output (nB or nA) propagation delays

Table 10. Measurement points

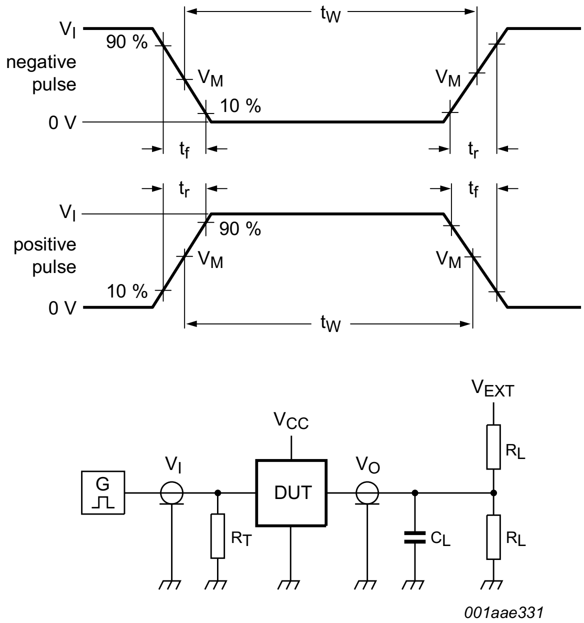
Supply voltage	Input			Output		
V_{CC}	V_M	V_I	$t_r = t_f$	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	V_{CC}	$\leq$ 2.0 ns	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	$\leq$ 2.0 ns	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 15. Enable and disable times



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	$2V_{CC}$
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	$2V_{CC}$

12.1 Additional dynamic characteristics

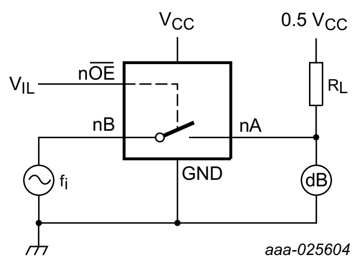
Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
$f_{(-3dB)}$	–3 dB frequency response	V_{CC} = 3.3 V; R_L = 50 Ω; see Figure 17 [1]	-	423	-	MHz

[1] f_i is biased at $0.5V_{CC}$.

12.2 Test circuits

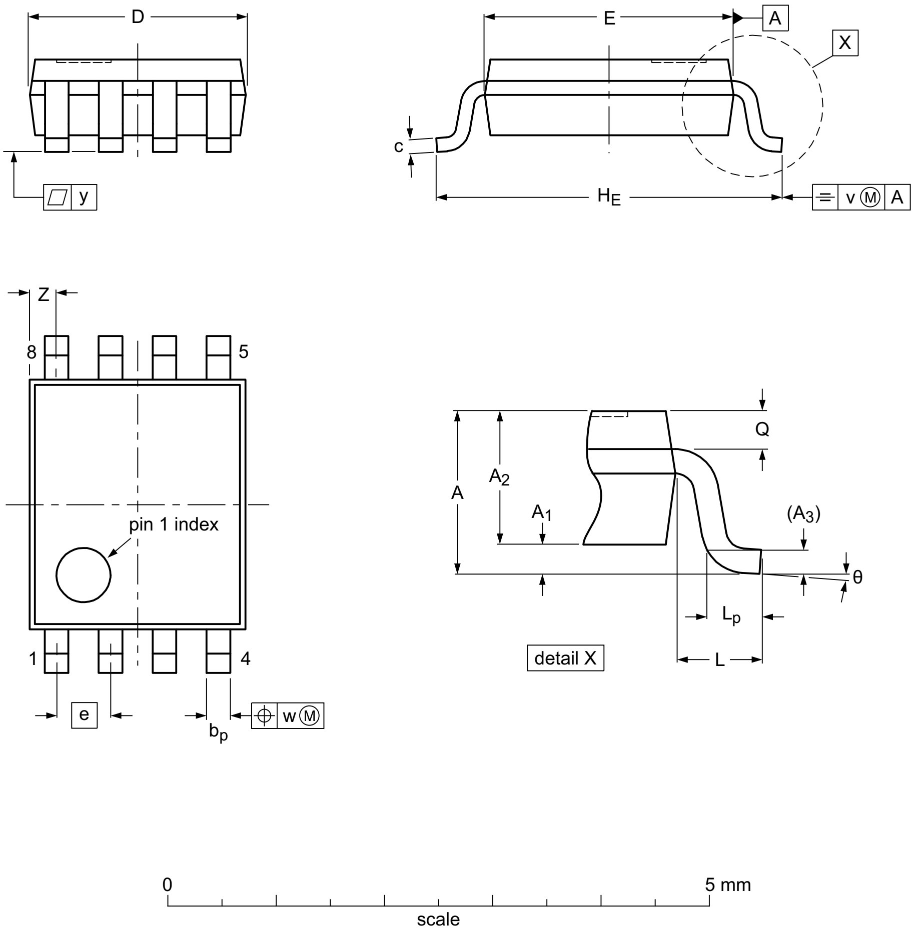


n$\overline{\text{OE}}$ connected to GND; Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads –3 dB.

Fig 17. Test circuit for measuring the frequency response when channel is in ON-state

13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit		A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
	nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

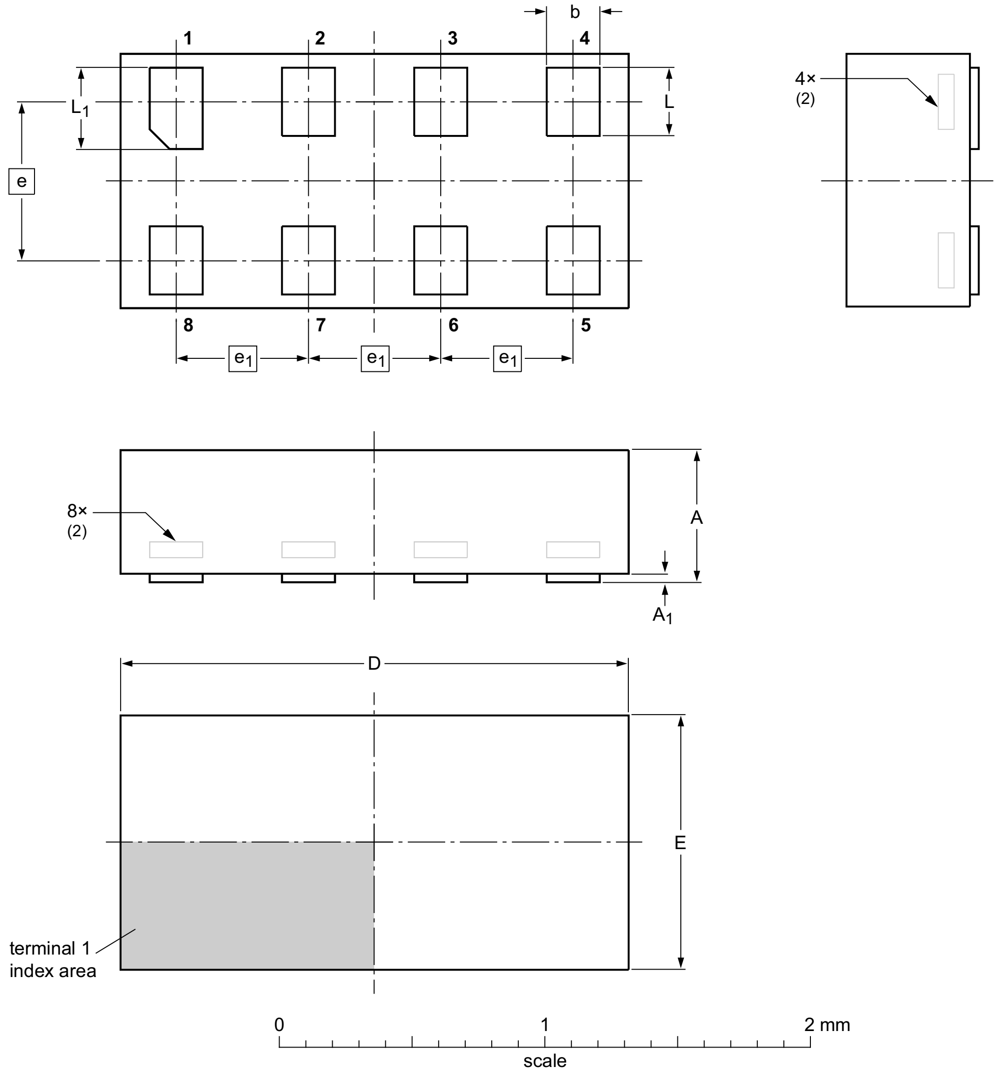
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig 18. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 19. Package outline SOT833-1 (XSON8)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3306 v.1	20161207	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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17. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

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