**General Description**

The MAX5039/MAX5040 provide intelligent control to power systems where two supply voltages need tracking. These cases include PowerPC®, DSP, and ASIC systems, which require a lower CORE voltage supply and a higher I/O voltage supply.

The MAX5039/MAX5040 control the output voltage of the CORE and I/O supplies during power-up, power-down, and brownout situations. They ensure that the two power supplies rise or fall at the same rate, limiting the voltage difference between the CORE and I/O supplies. This eliminates stresses on the processor. The MAX5039/MAX5040 shut down both the CORE and I/O supplies if either one is shorted or otherwise fails to come up.

The MAX5040 provides a power-OK (POK) signal that signals the processor if the CORE supply, the I/O supply, and the system bus supply (VCC) are above their respective specified levels. The MAX5039/MAX5040 are targeted for nominal bus VCC voltages from 4V to 5.5V. The MAX5039/MAX5040 work with CORE voltages ranging from 800mV to about 3V (depending on the gate-to-source turn-on threshold of the external N-channel MOSFET) and I/O voltages ranging from VCC to 4V. The MAX5039/MAX5040 provide tracking control of the I/O and CORE voltages using a single external N-channel MOSFET connected across them. This MOSFET is not in series with the power paths and does not dissipate any additional power during normal system operation. The external MOSFET is only on for brief periods during power-up/power-down cycling so a low-cost, small-size MOSFET with a rating of 1/4th to 1/8th of the normal supply current is suitable.

The MAX5039/MAX5040 are offered in space-saving 8-pin µMAX and 10-pin µMAX packages, respectively.

**Applications**

- PowerPC Systems
- Embedded DSPs and ASICs
- Embedded 16- and 32-Bit Controller Systems
- Telecom/Base Station/Networking

**Features**

- Provide Tracking of Two External Power Supplies During Power-Up and Power-Down
- Compatible with a Wide Range of External Power Supplies Independent of Output Power
- Bus Voltage Undervoltage Lockout Enables/Disables CORE and I/O Supplies Together
- Detect Short Circuit on V CORE and V I/O, Disable CORE and I/O Supplies in Either Case
- Output Undervoltage Monitoring
- POK Status (MAX5040)
- Operating VCC Supply Voltage Range: 2.5V to 5.5V
- I/O Voltage Range: V CORE to 4V
- CORE Voltage Range: 0.8V to V I/O

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX5039EUA-T</td>
<td>-40°C to +85°C</td>
<td>8 µMAX</td>
</tr>
<tr>
<td>MAX5040EUB-T</td>
<td>-40°C to +85°C</td>
<td>10 µMAX</td>
</tr>
</tbody>
</table>

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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim’s website at www.maxim-ic.com.
# Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

## ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>VCC</td>
<td>(Note 1)</td>
<td>2.5</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VCC Supply Current</td>
<td>Icc</td>
<td></td>
<td>1.3</td>
<td>2.25</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Lowest VCC Where SDO Is Valid</td>
<td>VCCLO</td>
<td>(Note 2)</td>
<td>0.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SDO Output Low Voltage at VCC = VCCLO</td>
<td>VUVLO = VCC = VCCLO, ISDO = 50μA, measure VSDO (Note 2)</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC IC Turn-On Voltage Threshold (Note 3)</td>
<td>VCC rising</td>
<td></td>
<td>2.43</td>
<td>2.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Core Voltage Range</td>
<td>VCORE</td>
<td>I/O and CORE valid, VCC = 5.5V (Notes 4, 5)</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V/I/O</td>
</tr>
<tr>
<td>I/O Voltage Range</td>
<td>VI/O</td>
<td>I/O and CORE valid (Note 5), 2.5V ≤ VCC ≤ 4V</td>
<td>VCC</td>
<td></td>
<td>VCORE</td>
<td></td>
</tr>
</tbody>
</table>

## ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Supply Conditions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Continuous Power Dissipation (TA = +70°C)**
- 8-Pin µMAX (derate 4.5mW/°C above +70°C) ......... 362mW
- 10-Pin µMAX (derate 5.6mW/°C above +70°C) ......... 444mW

## Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## USER-PROGRAMMABLE UNDERRANGE LOCKOUT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>UVLO Trip Threshold</td>
<td>VUVLO</td>
<td>VUVLO rising</td>
<td>1.200</td>
<td>1.230</td>
<td>1.260</td>
<td>V</td>
</tr>
<tr>
<td>Hysteresis</td>
<td></td>
<td></td>
<td>110</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

## CORE AND I/O REGULATION

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CORE Feedback, CORE_FB, and Reference Voltage</td>
<td>VCREF</td>
<td></td>
<td>784</td>
<td>800</td>
<td>816</td>
<td>mV</td>
</tr>
<tr>
<td>CORE Regulator Large-Signal Gain</td>
<td>AV</td>
<td>CORE_FB to NDRV</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>CORE Regulator Crossover Frequency</td>
<td>CORE_FB to NDRV</td>
<td>400</td>
<td></td>
<td></td>
<td>kHz</td>
<td></td>
</tr>
</tbody>
</table>

- **NDRV Output Resistance**
  - Pullup strength, V/I/O = 1V, VCORE = 2V, INDRV = -10mA
  - Pulldown strength, V/I/O = 2V, VCORE = 1V, INDRV = 10mA

- **I/O-CORE Comparator Trip Threshold (Note 6)**
  - VTH
  - VCORE - V/I/O, V/I/O falling
  - VCORE - V/I/O, V/I/O rising

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

ELECTRICAL CHARACTERISTICS (continued)

\((V_{CC} = 2.5V \text{ to } 5.5V, \ V_{UVLO} = 2V, \ V_{CORE} = 1.8V, \ V_{I/O} = 2.5V, \ V_{CORE\_FB} = 1V, \ V_{I/O\_SENSE} = 2V \text{ (MAX5040 only)}, \ TA = -40\degree \text{C to } +85\degree \text{C, unless otherwise specified. Typical values are at } V_{CC} = 5V, TA = +25\degree \text{C.)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regulator Amp Gain</td>
<td>AVOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td>CORE Pulldown Resistance</td>
<td>V_{CORE} = 1.8V, V_{UVLO} = 1V, V_{CC} = 2.5V</td>
<td>20</td>
<td>50</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>MONITOR OUTPUTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDØ Output Low Voltage</td>
<td>V_{OLSDO}</td>
<td>ISDØ = 1.8mA, V_{UVLO} = 1V, V_{CC} = 2.5V</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SDØ Output High Voltage</td>
<td>V_{OHSDO}</td>
<td>ISDØ = -1.0mA, V_{CC} = 4V</td>
<td>V_{CC} - V_{0.4V}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISDØ = -1.0mA, V_{CC} = 2.5V</td>
<td>V_{CC} - V_{0.55V}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O_SENSE Trip Threshold</td>
<td>V_{I/O_REF}</td>
<td>V_{I/O_SENSE} rising</td>
<td>1.200</td>
<td>1.230</td>
<td>1.260</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis</td>
<td>25</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>POK Output Low Voltage</td>
<td>V_{OLPOK}</td>
<td>IPOK = 1.8mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>POK Leakage Current</td>
<td>I_{POK}</td>
<td>VPOK = V_{CC}</td>
<td>1.0</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>POK Glitch Rejection Time</td>
<td>t_{POK}</td>
<td>(Note 7)</td>
<td>50</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Fault Time</td>
<td>t_{FAULT}</td>
<td>(Note 8)</td>
<td>10</td>
<td>15</td>
<td>20</td>
<td>ms</td>
</tr>
<tr>
<td>I/O and CORE INPUTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O Input Bias Current</td>
<td>V_{I/O} = 1V</td>
<td>V_{CORE} = 1V</td>
<td>20</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>CORE Input Bias Current</td>
<td>V_{CORE} = 1V</td>
<td>V_{CORE_FB} = 1.2V</td>
<td>20</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I/O_SENSE Input Bias Current</td>
<td>V_{I/O_SENSE} = 0.8V</td>
<td>V_{CORE_FB} = 1.2V</td>
<td>250</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>CORE_FB Input Bias Current</td>
<td>V_{CORE_FB} = 1.2V</td>
<td>V_{CORE_FB} = 1.2V</td>
<td>300</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

Note 1: \(V_{CC}\) slew-rate limited to 30V/µs.
Note 2: SDØ automatically goes low when the UVLO pin drops below its threshold (or \(V_{CC}\) drops below 2.5V). SDØ remains low as \(V_{CC}\) falls. For some \(V_{CC}\) below \(V_{CCLO}\) SDØ may float.
Note 3: This undervoltage lockout disables the MAX5039/MAX5040 at \(V_{CC}\) voltages below which the device cannot effectively operate. When \(V_{CC}\) drops below the threshold, SDØ goes low, the bleeder turns off, and POK is high impedance.
Note 4: In order to regulate correctly, \(V_{CC}\) must be higher than \(V_{CORE}\) plus the turn-on voltage of the external N-channel MOSFET.
Note 5: I/O and CORE valid mean the voltages on these pins have settled within their target specifications for normal operation.
Note 6: CORE and I/O supplies rise and fall rates must be limited to less than 6.6V/µs.
Note 7: POK does not deassert for glitches less than \(t_{POK}\).
Note 8: A fault condition is latched when either of the two following conditions maintains for longer than \(t_{FAULT}\):
   \(V_{CORE\_FB} < V_{CORE\_REF}\) (i.e., \(V_{CORE}\) is less than its set point)
   \(V_{I/O} < V_{CORE}\)
   A FAULT condition forces SDØ and POK (MAX5040 only) low. CORE discharges to GND through 20Ω while \(V_{CC} > 2.5V\). Cycle UVLO or \(V_{CC}\) low, then high, to clear a FAULT.
Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

Typical Operating Characteristics

(V_{CC} = 5V, V_{CORE} = 1.8V, V_{I/O} = 3.3V, T_A = +25°C, unless otherwise specified.)
Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

Typical Operating Characteristics (continued)

\( V_{CC} = 5V, V_{CORE} = 1.8V, V_{I/O} = 3.3V, T_A = +25^\circ C, \) unless otherwise specified.

![Graphs showing various electrical characteristics of MAX5039/MAX5040 controllers.](image-url)
## Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>MAX5039</th>
<th>MAX5040</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>SDO</td>
<td>Active-Low Shutdown Output. Connect SDO to active-low shutdown input of both CORE and I/O supplies. SDO is high when ( V_{UVLO} \geq V_{UVCC} ) and ( V_{CC} \geq 2.5V ) and if there is no fault.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>VCC</td>
<td>Supply Voltage Input. Connect VCC to the supply voltage that powers the CORE and I/O supplies. Bypass VCC to GND with a 1µF capacitor.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>UVLO</td>
<td>User-Programmable Undervoltage Lockout. Connect to midpoint of the voltage-divider from VCC to GND. Set trip point below minimum VCC voltage. ( V_{UVLO} \leq V_{UVCC} ) forces SDO and POK (MAX5040 only) low. Use UVLO as an active-low shutdown input to turn on/off the CORE and I/O supplies if desired.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>7</td>
<td>CORE_FB</td>
<td>CORE Feedback Input. Connect CORE_FB to the midpoint of the voltage-divider from CORE to GND. The MAX5039/MAX5040 keep CORE_FB from dropping below ( V_{C_REF} ) by controlling NDRV. Any time ( V_{CORE_FB} ) falls below ( V_{C_REF} ), NDRV rises above ground to a voltage sufficient to maintain ( V_{CORE_FB} = V_{C_REF} ). If ( V_{CORE_FB} ) remains below ( V_{C_REF} ) for longer than ( t_{FAULT} ), a latched FAULT is generated. During a FAULT, MAX5039/MAX5040 continue to regulate CORE_FB. Three things halt regulation of CORE_FB: • If VCC falls below 2.5V, NDRV goes to GND. • If I/O falls below CORE, NDRV goes to VCC. • If ( V_{CORE_FB} ) rises above ( V_{C_REF} ), NDRV goes to GND.</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>8</td>
<td>CORE</td>
<td>CORE Supply Sense Input. Connect CORE to the core output voltage. If ( V_{CORE} &gt; V_{I/O} ), NDRV goes to VCC. POK (MAX5040 only) goes low. FAULT is latched if this condition lasts longer than ( t_{FAULT} ). A 20Ω bleeder discharges CORE to GND whenever SDO is low and VCC &gt; 2.5V.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>9</td>
<td>I/O</td>
<td>I/O Supply Sense Input. Connect to I/O output voltage. If ( V_{CORE} &gt; V_{I/O} ), NDRV goes to VCC. POK (MAX5040 only) drives low. A FAULT is latched if this condition lasts longer than ( t_{FAULT} ).</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>10</td>
<td>NDRV</td>
<td>N-Channel MOSFET Gate Driver. Connect NDRV to the gate of the external N-channel MOSFET that shunts I/O to CORE.</td>
<td></td>
</tr>
<tr>
<td>—</td>
<td>5</td>
<td>I/O_SENSE</td>
<td>I/O Feedback Input. Use a resistor-divider to divide ( V_{I/O} ) and apply to this pin. When ( V_{I/O_SENSE} \leq V_{I/O_REF} ), POK drives low. I/O_SENSE can also be used to monitor any other voltage.</td>
<td></td>
</tr>
<tr>
<td>—</td>
<td>6</td>
<td>POK</td>
<td>Open-Drain Power-OK Output. POK drives low when any condition below is true: ( V_{CC} \leq 2.5V ), ( V_{UVLO} \leq V_{UVCC} ), ( V_{CORE_FB} \leq V_{C_REF} ), ( V_{I/O} \leq V_{CORE} ) ( V_{I/O_SENSE} \leq V_{I/O_REF} ), MAX5039/MAX5040 latches a FAULT.</td>
<td></td>
</tr>
</tbody>
</table>
Performance During Typical Operation

Scope shots are of the MAX5040 EV kit. Figures 1 through 8 demonstrate system performance of the MAX5040 under various power-up, power-down, and fault conditions. In some cases (described in detail below), startup or shutdown of the I/O and CORE supplies were purposely delayed with respect to each other to simulate possible system operating conditions.

In Figure 1 (with MAX5040), VCC ramps up slowly and the I/O supply comes up before the CORE supply. As soon as VCC rises above 2.5V (at about 7.5ms) NDRV goes to VCC shorting the I/O and CORE supplies together. When VCC rises above 4.5V (bringing VUVLO above VUVCC), SDO goes high enabling the I/O and CORE supplies. Although the CORE PWM supply turns on 5ms after the I/O PWM supply, both supply voltages come up together because NDRV is held at VCC, shorting the supplies together through the N-channel FET. The I/O supply supports both the I/O line and the CORE line. The CORE supply finally comes up (at around 7ms), then NDRV goes to VCC (at around 36ms), shorting the supplies together. NDRV remains at VCC until VCC falls below 2.5V and then it returns to GND.

In Figure 2 (without MAX5040), VCC ramps up slowly and the CORE and I/O supplies are turned on when VCC exceeds 2.5V. The I/O voltage comes up before the CORE voltage. There is a 3.3V difference between the I/O and CORE supplies for about 4ms before the CORE supply finally comes up. When VCC powers down, I/O remains high for about 10ms after CORE reaches GND.

In Figure 3 (with MAX5040), VCC ramps up slowly and the CORE supply comes up before the I/O supply. As soon as VCC rises above 2.5V (at about 7.5ms), NDRV goes to VCC, shorting the I/O and CORE supplies together. When VCC rises above 4.5V (bringing VUVLO above VUVCC), SDO goes high, enabling the I/O and CORE supplies. Although the I/O PWM supply turns on 8ms after the CORE PWM supply, both supply voltages come up together because NDRV is held at VCC, shorting the supplies together through the N-channel FET. The CORE supply supports both the CORE line and the I/O line until the I/O supply comes up. At around 23ms, the I/O supply turns on, pulling the I/O voltage above the CORE voltage. At this point, the MAX5040 brings NDRV to GND and POK goes high. On power-down, when VCC drops low enough to bring VUVLO below VUVCC, SDO immediately falls, turning the I/O and CORE supplies off. Simultaneously, POK falls, indicating power-down to the processor. When the CORE voltage drops below its regulation point, NDRV falls, indicating power-down to the CORE supply. When VCC powers down, the supplies do not turn off together. CORE remains high for around 14ms after I/O falls.

In Figure 4 (without MAX5040), VCC ramps up slowly and the CORE voltage comes up before the I/O voltage. It takes about 8ms before the I/O supply finally comes up above the CORE supply. When VCC goes high, enabling the I/O and CORE supplies. Although the CORE PWM supply turns on 5ms after the I/O PWM supply, both supply voltages come up together because NDRV is high, shorting the I/O and CORE supplies together. When VCC rises above 4.5V (bringing VUVLO above VUVCC), SDO goes high, enabling the I/O and CORE supplies. Both supplies come up together because NDRV is high. Note that the CORE supply is still off; CORE is held up through the N-channel FET shunt. Once VCC rises close to its set point, the linear regulator holds VCORE to its set point by regulating NDRV to around 2.8V. After 15ms of regulating CORE, the MAX5040 latches a fault. SDO goes low, NDRV goes to VCC, and both supplies power down together. POK remains low throughout because a valid operating state was not achieved.

In Figure 5 (with MAX5040), the system power-up is attempted with the CORE supply held in shutdown. As soon as VCC rises above 2.5V, NDRV goes to VCC, shorting the I/O and CORE supplies together. Next, when VCC rises above 4.5V (bringing VUVLO above VUVCC), SDO goes high, enabling the I/O and CORE supplies. Both supplies come up together because NDRV is high. Note that the CORE supply is still off; CORE is held up through the N-channel FET shunt. Once VCC rises close to its set point, the linear regulator holds VCORE to its set point by regulating NDRV to around 2.8V. After 15ms of regulating CORE, the MAX5040 latches a fault. SDO goes low, NDRV goes to VCC, and both supplies power down together. POK remains low throughout because a valid operating state was not achieved.

In Figure 6 (with MAX5040), VCC is set to 5V. Toggling UVLO from low to high controls system startup. While UVLO is low and the VCC is 5V, NDRV is high, causing the supplies to be shorted together. When UVLO goes high, SDO also goes high, turning on the CORE and I/O supplies (at around 3ms). In this example, the I/O supply comes up before the CORE supply. The MAX5040 regulates CORE by driving NDRV to about 2.8V until the CORE supply comes up (at around 7ms), then NDRV falls to GND and POK goes high. When UVLO is driven low, SDO goes low, disabling the CORE and I/O supplies. NDRV goes to VCC and both supplies power down together.

In Figure 7 (with MAX5040), VCC is set to 5V. Toggling UVLO from low to high controls system startup. While UVLO is low and the VCC is 5V, NDRV is high, causing the supplies to be shorted together. When UVLO is driven low, SDO goes low, disabling the CORE and I/O supplies. NDRV goes to VCC and both supplies power down together.
Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

supply. The MAX5040 holds up I/O by driving NDRV to VCC (because the I/O voltage is less than the CORE voltage) until the I/O supply comes up (at around 16ms). At this point, NDRV goes to GND and POK goes high. UVLO is driven low (at around 22ms), causing SDO to go low, disabling the CORE and I/O supplies. The CORE supply powers down at about 23ms and NDRV goes to 2.8V to regulate the CORE supply until I/O falls. Then NDRV goes to VCC when the I/O voltage falls to the CORE voltage (at around 36ms).

Figure 8 (with MAX5040) starts out with the supplies in their normal range. At 3ms, CORE is shorted to GND. NDRV goes high, and POK goes low immediately. NDRV shorts the I/O supply to the CORE supply, bringing the supplies down together. After 15ms, the MAX5040 latches a fault and SDO goes low turning off the supplies.

Detailed Description

The MAX5039/MAX5040 voltage-tracking controllers limit the maximum differential voltage between two power supplies during power-up, power-down, and brownout conditions. The devices provide a shutdown output control signal, SDO, which is used to turn on
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and off the CORE and I/O power supplies. The MAX5039/MAX5040 monitor and compare the CORE and I/O voltages as follows.

When the I/O voltage is greater than or equal to the CORE voltage, MAX5039/MAX5040 regulate the external N-channel MOSFET as a linear regulator by controlling NDRV. The linear regulator regulates the CORE voltage to the value set by the external resistor-divider connected from CORE to CORE_FB and GND (see Figures 9 and 10). If the CORE_FB voltage is far less than its regulation point, V_C_REF (800mV), NDRV drives high to VCC, effectively shorting CORE and I/O together through the external MOSFET. If the CORE_FB voltage equals V_C_REF, NDRV goes into regulation mode. If the CORE_FB voltage is higher than V_C_REF, the linear regulator goes into standby mode and pulls NDRV low, turning off the external N-channel MOSFET.

When the I/O voltage is lower than the CORE voltage by V_TH (90mV), the MAX5039/MAX5040 turn the external N-channel MOSFET on by driving NDRV high to VCC.

Whenever SDO is high, the MAX5039/MAX5040 track the time that NDRV is in regulation mode or driven high. If NDRV is in regulation mode or driven high for longer than t_FAULT (15ms), a fault occurs and SDO is pulled low.

Figure 5. System Power-Up/Power-Down, Fault Startup (CORE Supply Fails to Turn On)

Figure 6. System Turn-On/Turn-Off Under UVLO Control (V/I/O Rising Before VCORE)

Figure 7. System Turn-On/Turn-Off Under UVLO Control (VCORE Rising Before V/I/O)

Figure 8. Short-Circuit Response (CORE Shorted to GND)
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**Designing with MAX5039/MAX5040**

The MAX5039/MAX5040 provide intelligent control to power systems where two power supplies need tracking. Follow the steps below for designing with the MAX5039/MAX5040:

1) Select an appropriate external N-channel MOSFET (see the N-Channel MOSFET Selection section).
2) Set the CORE regulation voltage (see the Programming the CORE Voltage section).
3) Set the UVLO voltage trip threshold (see the Programming UVLO Voltage section).
4) Compensate the CORE linear regulator loop (see the Linear Regulator Compensation section).
5) Set the POK voltage trip threshold (MAX5040 only, see the Programming I/O_SENSE Voltage section).

Figures 9 and 10 show an application example.

**Functional Description**

SDO is the shutdown signal output. Connect SDO to the CORE and I/O power-supply shutdown pins. SDO allows the MAX5039/MAX5040 to control the turning on and off of the external switching regulators or linear regulators that supply the CORE and I/O voltages. Using this single control signal, the MAX5039/MAX5040 turn the CORE and I/O power supplies on and off together, minimizing the voltage differential between them.

SDO is low when:
- The voltage on the UVLO pin is below \( V_{UVCC} \) (1.230V).
- \( V_C \) is below the IC turn-on voltage threshold (2.43V).
- A fault condition is detected.

The MAX5039/MAX5040 prevent premature turn-on of the CORE and I/O power supplies during power-up by actively holding SDO low as soon as \( V_C \) rises above 0.9V, provided the condition for SDO to stay low is valid.

NDRV controls the gate of the external N-channel MOSFET (which is connected between the I/O and CORE voltages), as needed, as long as \( V_C \) is within its operating range.

NDRV is driven high to \( V_C \) when \( V_{I/O} < V_{CORE} \).

NDRV regulates the external MOSFET as a linear regulator when \( V_{I/O} > V_{CORE} \) and \( V_{CORE_FB} < V_{CORE_FB} < V_{C_REF} \).

NDRV is driven low when \( V_{I/O} > V_{CORE} \) and \( V_{CORE_FB} > V_{C_REF} \).
UVLO is a user-programmable undervoltage lockout input. When the UVLO voltage is above $V_{UVCC}$, the MAX5039/MAX5040 hold SDO high, given that $V_{CC}$ is within its operating range and there is no fault condition present. When the UVLO voltage falls below $V_{UVCC}$, SDO is pulled low. Use a resistor-divider from the input of the CORE and I/O power supplies to UVLO to GND to set the undervoltage lockout (see the Typical Application Circuit). The MAX5039/MAX5040 keep the CORE and I/O power supplies off (through the SDO) until their input voltage is within its operating range.

UVLO can be used to turn off the CORE and I/O power supplies through SDO. Pull the UVLO pin low with an open-collector driver to assert SDO, which turns off the power supplies.

**Active Bleeder**

The MAX5039/MAX5040 contain an internal 20Ω N-channel MOSFET bleeder that connects CORE to ground. The bleeder turns on whenever the MAX5039/MAX5040 hold SDO low and $V_{CC}$ is above the $V_{CC}$ IC turn-on voltage threshold (2.43V). This bleeder assists in discharging the output capacitor(s) during power-down/brownout conditions. The MAX5039/MAX5040 maintain tight voltage tracking of the CORE and I/O voltages, as long as $V_{CC}$ is within its operating voltage range. It is important to discharge the output capacitors to ground before $V_{CC}$ drops out of its range. Figure 11 illustrates a method to prolong $V_{CC}$ after a power-down/brownout condition.

The hold-up capacitor, $C_{HD}$, holds the voltage at $V_{CC}$ up and provides the power to the MAX5039/MAX5040 to keep them in operation even after $V_{IN}$ has gone down.

**Power-Up**

The MAX5039/MAX5040 prevent premature turning on of the CORE and I/O power supplies during power-up by actively holding SDO low as soon as $V_{CC}$ rises above 0.9V, provided the condition for SDO to stay low is valid. The MAX5039/MAX5040 completely turn on and NDRV is operational when $V_{CC}$ rises above the $V_{CC}$ IC turn-on voltage threshold (2.43V). In this state, the MAX5039/MAX5040 maintain tight tracking of the CORE and I/O output voltages. The MAX5039/MAX5040 continue to hold SDO low until the UVLO voltage rises above $V_{UVCC}$ (1.230V).

Once the UVLO voltage rises above $V_{UVCC}$, SDO goes high, enabling the CORE and I/O power supplies at the same time. Without voltage tracking, depending on the
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Without voltage tracking, depending on the output capacitance and loading, CORE and I/O voltages may not fall at the same rate. Similar to the power-up condition, the MAX5039/MAX5040 keep CORE and I/O voltages tracking together by controlling NDRV, dynamically driving NDRV high, low, or in regulation mode, depending on the CORE and I/O voltage condition.

During power-down/brownout, VCC is dropping and the UVLO voltage is also dropping. When the UVLO voltage falls below VUVCC, SDO is pulled low, disabling the CORE and I/O power supplies. Similar to the shutdown condition, the MAX5039/MAX5040 keep CORE and I/O voltages together. It is important that VCC remains in its operating voltage range in order to keep the MAX5039/MAX5040 operating to provide tracking until the output voltages have discharged to a safe level. Figure 11 illustrates a method to prolong VCC after a power-down/brownout condition. The bleeder circuitry is helpful in this power-down/brownout condition because the bleeder helps speed up the discharge process.

**FAULT Condition**

While SDO is high, the MAX5039/MAX5040 keep track of the time NDRV is driven high or in regulation mode. In a typical system during power-up, power-down/brownout, and normal operation, the time NDRV is driven high or in regulation mode should last for only a few milliseconds. If this time exceeds tFAULT (15ms), indicating an abnormal condition, a fault is generated. During a fault condition, SDO is driven low and NDRV continues its operation as described in the NDRV section.

A fault condition is latched. To clear a fault, toggle VCC and/or UVLO to unlatch and restart the system.

**Output Short-Circuit Condition**

If any of the outputs are shorted to ground, NDRV is driven high to keep the CORE and I/O voltages tracking each other. The current through the external MOSFET is limited by the current limit provided by the external power supply. If the short-circuit condition lasts more than tFAULT, a fault is generated, SDO is driven low (which turns off the CORE and I/O power supplies), and NDRV continues its operation as described in the NDRV section.

**Applications Information**

**N-Channel MOSFET Selection**

The external N-channel MOSFET connected between CORE and I/O power supplies is expected to turn on briefly during power-up and power-down/brownout conditions. During normal operation, this MOSFET is turned off. In general, only a small size MOSFET is needed. A MOSFET capable of carrying 1/4th to 1/8th

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**Normal Operation**

After the power-up period is over, CORE and I/O output voltages settle to their respective regulated values. The linear regulator formed by MAX5039/MAX5040 and the external MOSFET is turned off. During normal operation, the linear regulator goes into a standby mode and NDRV is driven low.

The resistor-divider from CORE to CORE_FB to GND must be set so that the linear regulator regulation voltage is less than the CORE power-supply regulation voltage. See the Programming the CORE Voltage section.

During normal operation, the MAX5039/MAX5040 constantly monitor the CORE, I/O, and CORE_FB voltages. NDRV responds as needed, according to the conditions described in the NDRV section.

**Power-Down/Brownout or Shutdown**

The MAX5039/MAX5040 continue to provide tracking for the CORE and I/O output voltages during power-down/brownout or shutdown.

During shutdown (UVLO is pulled below VUVCC), SDO is pulled low, disabling the CORE and I/O power supplies together. The CORE and I/O output voltages start to fall.

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**Figure 11. Circuit Prolongs VCC After a Brownout/Power-Down Condition**

The resistor-divider from CORE to CORE_FB to GND must be set so that the linear regulator regulation voltage is less than the CORE power-supply regulation voltage. See the Programming the CORE Voltage section.

During normal operation, the MAX5039/MAX5040 constantly monitor the CORE, I/O, and CORE_FB voltages. NDRV responds as needed, according to the conditions described in the NDRV section.
of the maximum output current rating of the CORE or I/O power supplies is adequate. However, care should be taken when selecting this MOSFET to make sure it is capable of sustaining all of the worst-case conditions, as well as riding through all of the fault conditions. The following are guidelines for selecting the external N-channel MOSFET:

1) MOSFET drain-to-source maximum voltage rating: $V_{DS}$ rating > $V_{I/O}$ maximum voltage.

2) MOSFET gate-to-source maximum voltage rating: $V_{GS}$ rating > $V_{CC}$ maximum.

3) MOSFET gate turn-on threshold voltage: $V_{GS(th)}$ < minimum operating voltage of ($V_{CC}$ - $V_{CORE}$). For example, if $V_{CC}$ minimum operating voltage is 4.5V, CORE voltage is 1.8V, then $V_{GS(th)}$ < (4.5V - 1.8V) = 2.7V. A MOSFET with logic-level gate turn-on threshold voltage is appropriate for this application.

4) Determine the maximum current that can go through the MOSFET during power-up, power-down/brownout, or output short-circuit conditions. In most cases, this maximum current is the current limit of the CORE or the I/O power supplies, whichever is larger. Choose the MOSFET with pulse current rating sufficiently higher than this current. Note that typical MOSFET pulse current rating is much larger than its continuous current rating.

5) Determine the MOSFET maximum $R_{DS(ON)}$ such that under worst-case current, the voltage drop across its drain-to-source is within the tracking limit (approximately 400mV for most PowerPCs, ASICs, and DSPs).

6) Determine the maximum single-shot power dissipation in the MOSFET during power-up, or during an output short-circuit condition. Considering the following cases:
   - During power-up, the CORE voltage comes up first, and the I/O power supply fails to turn on. The MOSFET turns on hard, keeping the I/O voltage close to the CORE voltage. The MOSFET in this case supports the I/O load current, as well as the charging of the I/O output capacitor. For most practical cases, the power charging the I/O output capacitor can be ignored. Since the I/O voltage never reaches its final value, the I/O load current might be off and the power dissipation in the MOSFET is minimal. However, assuming the worst-case condition that the I/O load draws its full-load current, the power dissipation in the MOSFET would be $I_{I/O}^2 \times R_{DS(ON)}$, where $I_{I/O}$ is the I/O full-load current.

7) Next, select the MOSFET that can take this single pulse energy without going over its maximum junction temperature rating. The maximum MOSFET junction temperature can be calculated as follows:

$$T_J = T_{AMB} + P_{PULSE} \times Z_{\theta JA}$$

where $T_J$ is the junction temperature, $T_{AMB}$ is the ambient temperature, $P_{PULSE}$ is the single-shot power dissipation calculated in step 6 above, and $Z_{\theta JA}$ is the junction-to-ambient thermal impedance of the selected MOSFET for a single pulse of $t_{FAULT}$ duration. $Z_{\theta JA}$ is specified in all typical MOSFET data sheets.

Example: $I/O$ = 3.3V, I/O power supply has a current limit ($I_{I/O}(LIM)$) of 6A, I/O full-load current is 3A. CORE is 1.8V, CORE power supply has a current limit ($I_{CORE}(LIM)$) of 6A, CORE full-load current is 4A. $V_{CC}$ = 5V + 0.5V. CORE and I/O voltages must track to within 400mV.

Choose a Si9428DY (N-channel MOSFET, $V_{DS}$ max = 20V, $R_{DS(ON)}$ at +25°C = 0.04Ω at $V_{GS}$ = 2.5V, $R_{DS(ON)}$ at +125°C = 1.5 x $R_{DS(ON)}$ at 25°C, from the MOSFET data sheet, $V_{GS}$ max = 8V).
From step 5: the maximum $V_{I/O}$ and $V_{CORE}$ differential voltage = $(I_{CORE(LIM)}) \times (R_{DS(ON)}) = 6A \times 0.04\Omega \times 1.5 = 360mV$.

From step 6 (first bullet): power dissipation = $I_{PSLIM}^2 \times R_{DS(ON)} = (6A)^2 \times 0.04\Omega \times 1.5 = 2.16W$.

From step 6 (second bullet): power dissipation = $(V_{I/O} - V_{CORE}) \times I_{CORE} = (3.3V - 1.8V) \times 4A = 6W$.

From step 6 (third bullet): power dissipation = $I_{I/O}^2 \times R_{DS(ON)} = (3A)^2 \times 0.04\Omega \times 1.5 = 0.54W$.

So, the worst-case power dissipation in the MOSFET is 6W for a maximum duration of 20ms. From the Si9428DY data sheet, under the normalized thermal transient impedance curve (Figure 12), the $Z_{\theta JA}$ is 0.05 x +70°C/W for a single pulse. The worst-case junction temperature of the MOSFET at +85°C ambient temperature is:

$$T_J = T_{AMB} + P_{DM} \times Z_{\theta JA} = +85°C + 6W \times 0.05 \times +70°C/W = +106°C$$

**Programming the CORE Voltage**

See the application circuit examples in Figures 9 and 10. The following explains constraints on the CORE voltage.

The high-side constraint requires that the CORE regulator maintain a minimum voltage during normal operation. The low-side limit requires that the CORE regulator hold the CORE voltage such that the voltage difference from I/O to CORE does not exceed the processor’s maximum allowable voltage difference:

To calculate the high-side limit, set the maximum CORE voltage set point at the minimum system CORE voltage minus the total system tolerance:

$$CORESET_{MAX} = COREMIN - TOL$$

$$\text{TOL} = \text{Total Tolerance}$$

Calculate the low-side constraint by taking the maximum system I/O voltage, subtracting the maximum allowable I/O to CORE difference and adding the total system tolerance.

$$CORESET_{MIN} = I_{OMAX} - \Delta V_{I/OC} + TOL$$

The following comprise the sources for the total system tolerance:

- Resistor resolution error
- Resistor tolerance error
- Resistor temperature drift (TCR) error
- MAX5039/MAX5040 reference error
- Loop-gain error

For example:

- $V_{CORE} = 1.800 \pm 5%$
- $V_{I/O} = 3.300 \pm 5%$
- Maximum voltage that I/O can exceed CORE without damage to the processor: $\Delta V_{I/OC} = (V_{I/O} - V_{CORE})_{MAX} = 2V$
- System minimum gain = 1000V/V
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Resistor tolerance error:

$$\text{ERROR}\text{RES-}\text{TOL}(\%) = \text{RES}_\text{TOL}(\%) \times 2 \times (1 - \text{Ratio})$$

where:

$$\text{Ratio} = \frac{\text{V}_\text{C\_REF}}{\text{V}_\text{REGNOM}} = \frac{800\text{mV}}{\text{V}_\text{REGNOM}}$$

If the nominal CORE set point is 1.6V, the ratio is 800mV/1600mV = 0.5. With 1% resistors, the resistor error is:

$$\text{ERROR}\text{RES-}\text{TOL}(\%) = \pm1\% \times 2 \times (1 - 0.5) = \pm1\%$$

Resistor temperature coefficient error:

A similar value applies when the (+) and (-) are reversed in the above quotient. TCR is expressed in parts per million. One-percent chip resistors are typically specified at ±100ppm while 0.1% resistors are specified at ±25ppm.

Resistor Resolution Error: This error can be negligible when R2 is split into two parts, a high-value 0.1% resistor in series with a low-value 1% resistor to trim the final value.

MAX5039/MAX5040 reference error: ±2.0% by specification.

Loop-gain error: This error is due to the finite system gain.

$$\text{ERROR}\text{GAIN} = 100 \left( \frac{A\text{OL} \times \text{Ratio}}{(A\text{OL} \times \text{Ratio}) + 1} - 1 \right)$$

A minimum but unspecified loop gain of 1000 yields a -0.2% gain error. No positive gain error is possible.

Calculate the maximum and minimum regulator core voltage set point as follows:

$$\text{CORE}_\text{SETMAX} = \text{COREMIN} - \text{TOL} = (1.8V - 5\%) - 2.5\% = 1.8V \times 92.5\% = 1.665V$$

$$\text{CORE}_\text{SETMIN} = \frac{\text{I/OMAX} - \Delta V\text{I/OCC} + \text{TOL}}{\text{R}2} = ((3.3V + 5\%) - 2V) + 2.5\% = (3.465V - 2V) \times 102.5\% = 1.465V \times 102.5\% = 1.5016V$$

Set the CORE voltage set point (V\_REGNOM) between 1.5016V and 1.665V and as close to the upper value (1.665V) as possible.

Connect the midpoint of a voltage-divider between CORE and GND to CORE\_FB, as shown in Figure 10. Set the midpoint voltage to 800mV for a maximum CORE voltage set point of 1.665V.

Choose a value for R1 of 10kΩ.

Calculate R2 with the following equation:

$$R2 = R1 \times \frac{\text{V}_\text{REGNOM} - 1}{\text{V}_\text{C\_REF}}$$

Example:

$$R2 = R1 \times \frac{\text{V}_\text{REGNOM} - 1}{\text{V}_\text{C\_REF}} = \left( \frac{0.8V}{1.665V - 0.8V} \right) 10k\Omega = 9.24855k\Omega$$

Using a standard 9.09kΩ (±0.1%) resistor in series with a 158Ω (1%) resistor yields negligible resolution error.

Programming UVLO Voltage

See the application circuit examples in Figures 9 and 10.

The MAX5039/MAX5040 provide a user-programmable undervoltage lockout feature through the UVLO pin. When using a resistor-divider, R7 and R8, from an input voltage rail (V\text{IN}) to UVLO to GND, the user-programmable UVLO feature allows V\text{IN} to get to a certain value before MAX5039/MAX5040 turn the system power supplies on together. V\text{IN} is usually the input voltage to the system power supplies and it can be the same as V\text{CC}. The UVLO pin also provides the system a way to turn on/off the system power supplies (see the UVLO section). Choose the UVLO trip point such that the minimum V\text{IN} voltage exceeds the maximum UVLO rising
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threshold. Follow the guidelines below to program the UVLO voltage:

1) Determine the VIN tolerance; ±5% is common.
2) Determine the VUVLO rising threshold tolerance:
   - Undervoltage lockout rising trip threshold, VUVCC, tolerance: 1.230V ±2.5%
   - Programming resistor tolerance: pick a ±1% resistor or better (±1.6% over temperature from Table 1)
   - Resistor-divider ratio tolerance: ±1% maximum for ±1% resistors
   - Resistor value resolution: ±0.5% (can be zero if exact resistor value is available)
   - Extra margin: ±1%
   Total = ±6.6%
3) Set VUVLO nominal value to:
   VIN nominal value - (VIN tolerance + VUVLO tolerance)
4) Calculate R7 using the equation:
   \[ R7 = \left( \frac{V_{UVLO_{nom}}}{V_{UVCC}} - 1 \right) R8 \]
   where R8 is typically 10kΩ.
   **Example:** VIN nominal value = 5V, VIN tolerance = ±5%; set the VUVLO nominal value to 5V - (5% + 6.6%) = 4.42V.
   Choose R8 = 10.0kΩ, ±1%:

   \[ R7 = \left( \frac{4.42V}{1.230V} - 1 \right) 10kΩ = 25.93kΩ \]
   Use the next-lower value: R7 = 25.5kΩ.

**Linear Regulator Compensation**

See the application circuit examples in Figures 9 and 10. The external MOSFET, together with the feedback resistor-divider, R1 and R2, from CORE to CORE_FB to GND, and NDRV form a linear regulator loop. This linear regulator should be compensated for stable operation.

**Note:** The linear regulator spends most of its time in idle mode. It operates in transient mode and regulation mode only during system power-up/power-down, brownout, and occasional system load transient conditions. Loop stability applies when the linear regulator is in the regulation mode. Follow these simple guidelines to stabilize the linear loop: (see the Core Regulator Loop Bode Plot in the Typical Operating Characteristics).

1) Place C1, a 100nF ceramic capacitor (X5R, X7R type or better) from NDRV to GND.
2) Select R1 and R2, a resistor-divider from CORE to CORE_FB to GND to set the linear regulator output regulation voltage (see the Programming Core Voltage section).
3) Place R3 and C2, an RC network from CORE_FB to NDRV. Set R3 = R1 and calculate C2 as follows:

   \[ C2 = \frac{1}{2\pi \times 10kHz \times R3} \]
4) Place R4, a preload resistor, from CORE to GND.
   Calculate R4 as follows:

   \[ R4 \leq \frac{V_{CORE}}{0.03A} \]
5) Place R9 and C3, a lead network, from VCORE to CORE_FB. Set R9 = R1/10, and calculate C3 as follows:

   \[ C3 = \frac{1}{2\pi \times 7227Hz \times R9} \]

**Example:** CORE power supply = 1.8V, VREGNOM = 1.6V, C_{CORE} = 100μF, Q1 = Si9428 (Vishay Siliconix):

   \[ R1 = R3 = 10.0kΩ, 1% \]

   \[ C2 = \frac{1}{(2\pi \times 10kHz \times 10kΩ) \times 1.6nF} = 1.6nF \]

   Use a 1.5nF standard value.

   \[ R4 \leq \frac{1.6V}{0.03A} = 53Ω \]

   Use a 51Ω standard value.

   \[ C3 = \frac{1}{2\pi \times 7227Hz \times R5} = \frac{1}{2\pi \times 7227Hz \times 1kΩ} = 22nF \]
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Programming I/O_SENSE Voltage (MAX5040 Only)

See the application circuit examples in Figures 9 and 10. I/O_SENSE is used to monitor the I/O output voltage or any other voltage. The result is reported by the POK output signal. Choose the I/O_SENSE trip point such that the minimum monitored voltage at I/O_SENSE exceeds the maximum I/O_SENSE rising threshold.

Follow the guidelines below to program the I/O_SENSE voltage:

1) Determine the tolerance of the output voltage to be monitored, V_O: 5% is common.

2) Determine V_I/O_SENSE rising threshold tolerance:
   - I/O sense trip-point threshold, V_I/O_REF, tolerance: 1.230V ±2.5%
   - Resistor error tolerance build-up is the same as that calculated in the Programming UVLO Voltage section.
   - Total = ±6.6%.

3) Set V_I/O_SENSE rising nominal value to: V_O nominal value - (V_O tolerance + V_I/O_SENSE tolerance).

4) Calculate using the following equation:

   \[ R_5 = \left( \frac{V_{I/O\_SENSENOM} - 1}{V_{I/O\_REF}} \right) R_6 \]

where R6 is typically 10kΩ.

Example: V_{I/O} nominal value = 3.3V, set V_{I/O\_SENSENOM} nominal value to 3.3V - (5% + 6.6%) = 2.9172V.

Choose R6 = 10.0kΩ, 1%:

\[ R_5 = \left( \frac{2.9172V}{1.230V} - 1 \right) 10k\Omega = 13.72k\Omega \]

Use the next lower 13.7kΩ standard value.

Calculating Component Values

For more detailed information, go to Maxim’s website for the Application Note, "Dual Voltage Tracking Circuit for I/O, Microprocessor, and DSP Core Voltages." A link in the application note has a downloadable component selection spreadsheet for calculating component values. This spreadsheet calculates values for all passive components in Figure 10 and lists the resulting min/max values of VREGNOM for standard PowerPC core voltages. DIY options are included for other core and I/O voltages.
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Typical Operating Circuit

Pin Configurations

Chip Information

TRANSISTOR COUNT: 1272
PROCESS: BiCMOS
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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

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<tr>
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</tr>
<tr>
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<td>S</td>
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Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

NOTES:
1. DAE DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.